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MENDELSOHN & ASSOCIATES, P.C.
1500 JOHN F. KENNEDY BLVD., SUITE 405
PHILADELPHIA, PA 19102

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KIM, DAVID S	

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REQUEST FOR RECONSIDERATION/OTHER

Continuation of 11. does NOT place the application in condition for allowance because:

Applicant's arguments have been considered, but they are not persuasive. Applicant presents three salient points.

Regarding the first point, Applicant states,

> Claim 1 recites, inter alia, the steps of: (i) **integrating** the electrical signal **over a** first sampling **window** to generate a first integration result and (ii) **integrating** the electrical signal **over a** second sampling **window** to generate a second integration result.
>
> In the rejection of claim 1, the Examiner cites and relies on Figure 4 of Moeller-022 as teaching the above-specified limitations of the claim. In particular, the Examiner states that "integration for the left [and right] sampling point is implied in the decision circuit 240." For the following reasons, the Applicants submit that the above-specified limitations of claim 1 are non-obvious over the cited teachings of Moeller-022.
>
> Inspection of Moeller-022 reveals that it describes its processing method by consistently and repeatedly using the phrases like "sampling **point**" and "signal is sampled at [a] **point**" (see, e.g., paragraphs [0024] and [0027]). Nowhere does Moeller-022 use the phrase "integrating over a sampling window" or the terms "integrating" and "sampling window." Yet, the Examiner somehow concludes that Moeller-022 teaches or reasonably suggests integrating a signal over a sampling window.
>
> As known in the art, the term "sampling" refers to a process of converting a continuous signal into discrete data. The term "point sampling" designates a process of obtaining a value of the continuous signal at a particular fixed instant (i.e., point) in time. Although technical limitations of a real-life electronic circuit usually cause it to have a finite time resolution, an electronic circuit adapted for "point sampling" is normally designed to generate signal samples that approximate the ideal point samples as closely as practically possible. The latter means that the characteristics of the electronic circuit are chosen so that the signal does not significantly change while a sample of the signal is being generated by the electronic circuit.
>
> In contrast, an electronic circuit adapted for signal integration is designed to generate a signal sample that represents an integral of the signal over a time interval, and not just a point sample of the signal. A typical purpose of integrating a signal is to obtain its average value over the sampling-window duration or to smooth out undesirable (e.g., noise-induced) signal fluctuations. This means that the duration of the sampling window is normally chosen so that the signal is able to change or fluctuate significantly within the sampling window. Clearly, **sampling** a signal **at a point** and **integrating** a signal **over a** sampling **window** are two **very different** signal processing techniques because the former aims at obtaining a snap-shot of the signal while the latter allows the signal to evolve while being measured. It is therefore submitted that the Examiner's contention that signal integration can be implied from point sampling of the signal is unfounded and improper.
>
> For all these reasons, it is submitted that the Examiner's contention that Moeller-022 teaches or reasonably suggests the limitation of "integrating the electrical signal over a [first or second] sampling window" is unfounded and improper. It is therefore submitted that Moeller-022 does not provide an adequate basis for, and therefore cannot support, the conclusion of obviousness with respect to these limitations of claim 1.

(REMARKS, section "Steps of Integrating" on p. 2-3, emphasis Applicant's).

Examiner respectfully notes and appreciates Applicant's discussion of "point sampling" and "signal integration". However, Examiner respectfully notes that Moeller-022 does not disclose the relatively narrow process of "point sampling", as explained by Applicant. Rather, Moeller-022 more broadly discloses an "optical signal is ***sampled at*** more than one ***point***" (e.g., paragraph [0027]). Accordingly, Moeller-022 is not limited to the scope of Applicant's discussion of "point sampling". Similarly, Examiner respectfully notes that the claim language does not disclose the relatively narrow process of "signal integration", as explained by Applicant. Rather, the claim language more broadly discloses "***integrating*** the electrical ***signal*** over a…sampling window to generate a…integration result" (claim 1). Accordingly, the claim language is not limited to Applicant's discussion of "signal integration".

Clearly, a real-life application of Moeller-022's "sampling" would be taken over a finite amount of time. Moeller-022 employs the term "point" to describe this finite amount of time. However, since a finite amount of time has a start and an end, one may also describe this finite amount of time as a "window", which has a start and an end. Moeller-022 is relatively silent about the length of this finite amount of time. However, Moeller-022 does show that this finite amount of time is short enough to fit two instances into one bit slot (two sampling points in the bit slot of Fig. 4).

Similarly, a real-life application of Applicant's claim 1 "integrating" would be taken over a finite amount of time (M1 and M2 in Fig. 3A). Applicant employs the term "window" to describe this finite amount of time. However, since this finite amount of time also occurs at a particular location in time, one may also describe this finite amount of time as a "point", which also occurs at a particular location in time (e.g., the location of M1 and M2 in time in Fig. 3A). Applicant is relatively silent about the length of this finite amount of time, except for disclosing "relatively short sampling windows". For example, Applicant does show that this finite amount of time is short enough to fit two instances into one bit slot (e.g., M1 and M2 in Fig. 3A).

Moreover, Applicant's disclosure does not limit the "shortness" of these "relatively short sampling windows". Therefore, Applicant's "integrating" may include the scope of very short sampling windows, e.g., very narrow "points" in time. Due to the similarity and overlap in scope of these teachings of Moeller-022 and Applicant's disclosure regarding "sampling" over a finite amount of time, one may read

Moeller's "sampling point" as Applicant's claim 1 "integrating over a sampling window". Accordingly, this point is not persuasive.

Regarding the second point, Applicant states,

> Claim 1 further recites the limitation of **a duty cycle greater than one**.
> The Examiner finds this limitation obvious based on the combination of Moeller-022 and Singh. More specifically, the Examiner states that claim 9 in Moeller-022 recites non-return-to-zero (NRZ) pulses. The Examiner further states that Singh discloses NRZ pulses that are "on for an entire period," which corresponds to a duty cycle of one, and that Singh further discloses pulse broadening due to dispersion in the optical fiber, which is capable of increasing the duty cycle to greater than one. The Examiner then concludes that, based on Singh, "one would expect NRZ pulses received by Moeller to [possibly] have a duty cycle greater than one."
> While it is true that Singh discloses NRZ pulses that are "on for an entire period" and that those pulses can be broadened by dispersion in the optical fiber, the Applicants submit that these teachings alone are not sufficient to render the above-specified limitation of claim 1 obvious over the combination of Moeller-022 and Singh. Rather, the conclusion of obviousness hinges on the question of whether it would have been obvious to one of ordinary skill in the art to apply the method disclosed in Moeller-022 to an NRZ signal having a duty cycle greater than one disclosed by Singh. For the following reasons, the Applicants submit that it would not have been obvious to one of ordinary skill in the art to apply the method disclosed in Moeller-022 to the NRZ signal disclosed by Singh, notwithstanding the Examiner's assertions to the contrary.
> First of all, the Applicants note that the exact language of Moeller-022's claim 9 is as follows: "The method of claim 8, wherein said input optical signal is a non-return-to-zero (NRZ) optical pulse." Thus, it is clear that Moeller-022's claim 9 only specifies the type of the optical signal (which is NRZ) but does not specify its duty cycle. In fact, inspection of the entire specification in Moeller-022 reveals that the term "duty cycle" is not mentioned there at all. The only examples in Moeller-022 from which the duty cycle can be inferred are shown in Figs. 1, 3, and 4. More specifically, the example shown in Fig. 1 has a label "10 Gb/s 33% RZ TX," the most reasonable interpretation of which is that it refers to a return-to-zero (RZ) signal having a duty cycle of 33% (or 0.33). The duty cycle for the examples shown in Figs. 3 and 4 can be estimated as a ratio of the pulse width to the bit-slot width. That ratio and therefore the duty cycle does not exceed 50% (or 0.5) by any measure. Thus, Moeller-022 does not explicitly teach or implicitly suggest that its method can be applied to process an optical signal having a duty cycle greater than one.
> Second, the Applicants note that, by definition, an NRZ signal is a signal that does not fall to a zero level between two adjacent "ones." The NRZ signal does fall to the zero level when the bit sequence that it represents has a binary "zero." The Applicants further note that the NRZ designation alone does not say anything about the duty cycle of the signal and, certainly, does not automatically mean that the signal has a duty cycle of at least one. For example, it is clear that the concept of "duty cycle" does not apply to a continuous sequence of NRZ "ones" because it is practically impossible to tell where the preceding "one" ends and the next "one" begins. However, the duty cycle of an NRZ signal can still be inferred from the position of the transition edge between a "zero" and an adjacent "one." In particular, the Applicants submit that, in an optical NRZ signal having a duty cycle greater than one, the transition edge between an optical "zero" and an adjacent optical "one" is located inside the bit interval corresponding to the "zero."
> Finally, the Applicants note that the method of Moeller-022 is aimed at reducing the number of jitter-induced decoding errors (see, e.g., Moeller-022's paragraphs [0002] and [0007] and claims 1 and 14). For an NRZ signal having a duty cycle greater than one, the effect of jitter is to randomly change the position of the transition edge between an optical "zero" and an optical "one" within the bit interval corresponding to the optical "zero." This random position variation creates a probability for at least one of the two sampling points inside the "zero" bit interval to

> overlap with the transition edge and cause decision circuit **240** to output a "one," instead of a "zero," as a corresponding sample of the signal. An "OR" function applied to a bit combination having at least one "one" returns a "one," which represents a decoding error for the optical "zero." Thus, if applied to an optical NRZ signal having a duty cycle greater than one, the method of Moeller-022 would increase, rather than decrease, the number of jitter-induced decoding errors due to the additional decoding errors in the "zero" bit intervals. Since the aim of the method of Moeller-022 is exactly the opposite of this result, the Applicants submit that one of ordinary skill in the art would not be motivated to apply the method of Moeller-022 to NRZ signals having a duty cycle greater than one.
>
> For all these reasons, the Applicants submit that the Examiner improperly combined Moeller-022 and Singh to reject claim 1 and that this rejection should be withdrawn. It is further submitted that the above-specified "duty cycle" limitation of claim 1 is non-obvious over Moeller-022 and Singh.
>
> (REMARKS, section "Duty Cycle Greater Than One", p. 3-4, emphasis Applicant's).

Examiner respectfully notes and appreciates Applicant's discussion of the ***obviousness*** of applying the method disclosed in Moeller-022 to the NRZ signal disclosed by Singh. However, notice that the incorporation of teachings from Singh are ***not*** applied in an obviousness argument. That is, Singh is applied as a reference, like a dictionary, to provide more detailed information about teachings in Moeller-022 (e.g., see MPEP 2131.01 Multiple Reference 35 U.S.C. 102 Rejections). In other words, the standing rejections do ***not*** rely on an obviousness argument to combine the teachings of Singh with the teachings of Moeller-022. Accordingly, Applicant's discussion of the obviousness of applying the method disclosed in Moeller-022 to the NRZ signal disclosed by Singh is moot.

More exactly, notice that Moeller-022 ***already*** positively teaches the use of an NRZ signal (Moeller-022, claim 9). Singh shows that an NRZ signal, by definition, is "on for an entire period" of a bit slot, i.e., a duty cycle equal to one. Singh also shows that pulses generally undergo broadening in optical fiber (Singh, "Handling Impairments"). Moeller-022 shows the propagation path to be fiber (e.g., "transmission fiber" in paragraph [0019]). Accordingly, ***without*** any consideration of obviousness, one would expect the NRZ signal of Moeller-022 to experience pulse broadening, which would result in a duty cycle greater than one. Therefore, this point is not persuasive.

Regarding the third point, Applicant states,

> Claim 1 further recites the step of applying an **"AND" function** to the first and second bit estimate values to generate a bit of the bit sequence.
>
> In the rejection of claim 1, the Examiner admits that Moeller-022 "does not expressly disclose" this step. However, on page 4, the Examiner asserts that:

> Rather, Moeller discloses the application of an "OR" function (e.g., gate 260 in Fig. 2, gate 570 in Fig. 5) [and] the option of applying other alternative circuitry (paragraph [0020]). The usage of the "OR" function is to reduce the error probability for logical "1" values (paragraph [0027]). Logically speaking, an "AND" function is an "OR" function for "0" values. That is, a regular "OR" function outputs a "1" if any input is "1". Similar in operation, a regular "AND" function outputs a "0" if any input is a "0". At the time the invention was made, it would have been obvious to one of ordinary skill in the art to notice that such similar operation is an obvious variation of the method of Moeller. One of ordinary skill in the art would have been motivated to employ an "AND" function for the similar reason of employing an "OR" function, i.e., to reduce the probability of a particular bit estimate value, e.g., "0" values.

First, the Applicants submit that, as correctly noticed by the Examiner in the above-cited passage, changing the application of an "OR" function to the application of an "AND" function requires a recognition of the fact that incorrect decoding of optical "zeros," rather than optical "ones," can be a major source of decoding errors. However, that **recognition is absent** in Moeller-022 because Moeller-022 primarily deals with decoding of optical return-to-zero (RZ) signals having a relatively small duty cycle, e.g., about 33% (see, e.g., Moeller-022's Figs. 3-4 and paragraphs [0018]-[0019]). When an optical signal has a small duty cycle, transmission impediments, such as jitter, do not increase the error probability for optical "zeros" (see, e.g., the last sentence of Moeller-022's paragraph [0026]). Therefore, there is no problem of incorrect decoding of optical "zeros" in Moeller-022, and this problem is not recognized there. In contrast, the present application recognized that, for optical signals broadened by dispersion and/or having a relatively large duty cycle, e.g., about 100%, incorrect decoding of optical "zeros" can be a major source of decoding errors (see, e.g., Applicants' Figs. 3A and 4A-B and page 5, lines 1-5).

Second, the Applicants submit that Moeller-022 does not expressly suggest applying logical functions other than the "OR" function, notwithstanding the Examiner's statement to the contrary. More specifically, the relevant portion of relied-upon by the Examiner paragraph [0020] in Moeller-022 reads as follows:

> Although the front-end pre-amplified receiver **200** of FIG. 2 is depicted as a relatively complex receiver, a less complex conventional front-end pre-amplified receiver can also be implemented within various embodiments of the present invention. Additionally, **although** the logic circuitry **260** of FIG. 2 is **depicted as an OR logic gate, other circuitry** or devices that are **able to determine a resulting logic state** of at least one input signal **can be implemented** with the concepts of the present invention. [Emphasis added.]

It is clear from the context of paragraph [0020] that what is being discussed here is **different hardware implementations of the same logic functionality**, and **not a different logic functionality** as implied by the Examiner. Indeed, the first of the above-cited sentences talks about replacing relatively complex front-end pre-amplified receiver **200** by a less complex receiver capable of performing the same function as receiver **200**. Likewise, the second of the above-cited sentences talks about **replacing an OR logic gate with a different circuit capable of performing the same logic function as the OR gate**. The Applicants submit that reading a suggestion of a logic function change into the above-cited text is unwarranted.

Finally, and perhaps most importantly, changing the "OR" functionality of logic circuitry **260** to a different logic functionality, e.g., the "AND" functionality, would increase, rather than decrease, the number of decoding errors in receivers disclosed in Moeller-022 (see, e.g., Moeller-022's Fig. 4). More specifically, the two signal samples shown in Moeller-022's Fig. 4 will cause decision circuit **240** to output a "zero" for the left sample and a "one" for the right sample. An "AND" function applied to a "zero-one" combination returns a "zero." The latter represents a decoding error for the signal shown in Moeller-022's Fig. 4. The Applicants submit that a modification or variant that would actually worsen the performance of the device cannot be properly read into the device description or assumed obvious to one of ordinary skill in the art.

> To summarize, Moeller-022 (1) does **not** recognize that incorrect decoding of optical "zeros," rather than optical "ones," can be a major source of decoding errors and (2) does **not** suggest an application of a logical function other than the "OR" function for the purpose of correcting jitter-induced decoding errors. The Applicants submit that, in the absence of such recognition or suggestion, it would not have been obvious to one of ordinary skill in the art to change an "OR" function in Moeller-022 to an "AND" function recited in claim 1, notwithstanding the Examiner's assertion to the contrary.
>
> (REMARKS, section “Step of Applying an AND Function”, p. 4-5, emphasis Applicant’s).

Examiner respectfully notes that claim 1 of Moeller-022 suggests a ***broader*** use of logic as the invention of Moeller-022 as no mention of an OR gate appears in the claims until dependent claim 11 of Moeller-022. Although an OR logic function is expressly disclosed, the contextual principles of Moeller-022 do not appear to exclusively limit the logic function to that of an OR logic function.

In response to Applicant’s discussion about “changing the application of an ‘OR’ function to the application of an ‘AND’ function requires a recognition of the fact that incorrect decoding of optical ‘zeros,’ rather than optical ‘ones,’ can be a major source of decoding errors” and “that recognition is absent”, Examiner respectfully notes that such a specific scope of recognition is ***included*** in the ***broad*** range of considerations of Moeller-022. Examiner respectfully notes that the scope of the invention of Moeller-022 is ***broader*** than the specific examples provided (e.g., Fig. 4). For example, paragraph [0017] states that "the inventive concept can be advantageously implemented in various other transmission systems wherein it is desirable to improve a jitter tolerance". The specific example provided by Moeller-022 is that of properly detecting a logical "one" value (i.e., Fig. 3) represented by a return-to-zero (RZ) pulse. However, jitter tolerance is not concerned with “one” values or “zero” values, per se. Rather, the focus of jitter tolerance is to provide correct decoding of ***any*** desired value in the presence of jitter. Accordingly, implementing jitter tolerance would recognize that incorrect decoding of ***any*** value, “one” or “zero”, due to jitter, would be a major source of decoding errors. Moeller-022 addresses the ***broad*** concept of improving a jitter tolerance, and so would include the scope of recognizing that incorrect decoding of ***any*** value, “one” or “zero”, due to jitter, would be a major source of decoding errors.

In response to Applicant’s discussion about “Moeller-022 does not expressly suggest applying logical functions other than the ‘OR’ function, notwithstanding the Examiner's statement to the contrary”, Examiner points out the following:

> Although the front-end pre-amplified receiver 200 of FIG. 2 is depicted as a relatively complex receiver, a less complex conventional front-end pre-amplified receiver can also be implemented within various embodiments of the present invention. Additionally, although the logic circuitry 260 of FIG. 2 is depicted as an OR logic gate, *other circuitry or devices that are able* ***to determine a resulting logic state*** *of at least one input signal can be implemented* ***with the concepts of the present invention*** (Moeller-022, paragraph [0020], emphasis Examiner's).

Applicant reads the highlighted portion as "the second of the above-cited sentences talks about replacing an OR logic gate with a different circuit capable of performing the ***same*** logic function as the OR gate". However, the actual text is not so ***narrow***. Rather, the text states, "*other circuitry or devices that are able* ***to determine a resulting logic state*** *of at least one input signal can be implemented* ***with the concepts of the present invention***". "[T]o determine a resulting logic state" is broader than Applicant's reading of "replacing an OR logic gate with a different circuit capable of performing the ***same*** logic function as the OR gate". Also, as noted above, the "concepts of the present invention" address the ***broader*** issue of jitter tolerance, not just the ***specific*** example of Fig. 4 of Moeller-022 employing the OR gate of Fig. 2 of Moeller-022. Moreover, again, Examiner respectfully notes that claim 1 of Moeller-022 suggests a ***broader*** use of logic as the invention of Moeller-022 as no mention of an OR gate appears in the claims until dependent claim 11 of Moeller-022. Although an OR logic function is expressly disclosed, the contextual principles of Moeller-022 do not appear to exclusively limit the logic function to that of an OR logic function.

In response to Applicant's discussion about "changing the 'OR' functionality of logic circuitry **260** to a different logic functionality, e.g., the 'AND' functionality, would increase, rather than decrease, the number of decoding errors in receivers disclosed in Moeller-022 (see, e.g., Moeller-022's Fig. 4)", Examiner respectfully notes that the standing rejection does not rely on the specific scenario shown in Moeller-022's Fig. 4. That is, the specific scenario of Moeller-022's Fig. 4 shows an ***RZ signal***. Applicant's conclusion of an increase in the number of decoding errors relies on characteristics of an RZ signal. However, the standing rejection relies on an ***NRZ signal*** (NRZ pulses in claim 9 of Moeller-022). Due to the characteristics of an NRZ signal, using an AND function would not increase the number of decoding errors. Accordingly, this point is not persuasive.

Summarily, Applicant's arguments are not persuasive. Accordingly, Examiner respectfully maintains the standing rejections.

Additionally, Examiner presents the following discussion to further explain the obviousness argument presented in the standing rejection of claim 1.

In the field of logic processing, it is an extremely common and obvious practice to consider ***inverse*** scenarios since inverse scenarios provide ***equivalent*** functionality with ***alternate logic values*** (e.g., changing "one" values to "zero" values and vice versa). An inverse scenario to the example of Moeller-022 could be that of properly detecting a "zero" value, represented by a notch or "valley" between two neighboring "plateaus" of high value (e.g., invert Fig. 4 of Moeller-022 by simply turning it upside-down). Whereas the express example of Moeller-022 focuses on decreasing the error probability for "ones", an ***inverse*** scenario could focus on decreasing the error probability for "zeros". In view of such considerations, the OR logic function in the express example of Moeller-022 would provide the ***equivalent*** inventive functionality as that of an AND logic function in an ***inverse*** scenario. The rationale for using either logic function would be the ***same***: to reduce the error probability for a particular bit estimate value, i.e., "one" values for the express example of Moeller-022 and "zero" values for an inverse scenario, resulting in improved performance for each respective scenario.

Moreover, Applicant appears to express the same opinion of obviousness of different scenarios in the following admission from Applicant's own specification:

> The choice of logical function applied to the bit estimate values corresponding to sampling windows M1 and M2 is primarily determined by the type of error-causing impediment to the optical signal. For example, as already indicated above, for the eye diagram of Fig. 3A, most decoding errors are related to false binary "ones" attributed to waveform 304. In this situation, the "AND" function is an appropriate function choice because it returns a "0" whenever at least one of the bit estimate values is "0". In a different situation, e.g., when most decoding errors are related to false binary "zeros" attributed to waveform 302, the ***"OR"*** function would be an appropriate function choice. ***One skilled in the art will appreciate that, depending on the type of impediment and/or waveform shape, other logical functions or other numbers (e.g., three or more) of sampling windows may similarly be employed***. For example, the present invention may be implemented with three sampling windows, wherein (i) an "OR" function is applied to the bit estimate values corresponding to two of these sampling windows and (ii) an "AND" function is applied to the bit estimate value corresponding to the third sampling window and the value returned by the "OR" function to produce the final bit value to be output from the decoder.

(Applicant's specification, p. 6, l. 17-30, emphasis Examiner's).

Applicant admits that one skilled in the art will appreciate different variations, including "other logical functions", to address different scenarios, including different "type[s] of impediment[s] and/or waveform shape[s]". Such sentiments are within the spirit of Moeller-022's broad range of considerations of improving jitter tolerance, as noted above. Applicant even notes the same specific scenario employed by Moeller-022, i.e., the "OR" function to address false binary "zeros". As Applicant admits that one skilled in the art will appreciate different variations, in view of Applicant's variation of employing an "OR" function to address false binary "zeros", it similarly follows that one skilled in the art will appreciate different variations, in view of Moeller-022's same variation of employing an "OR" function to address false binary "zeros".

Accordingly, the obviousness argument presented in the standing rejection of claim 1 addresses the particular and obvious variation of considering an ***inverse*** scenario (i.e., employing an "AND" function to address false binary "ones"), which provides ***equivalent*** functionality with ***alternate logic values***, as is common and obvious in the field of logic processing.

/Kenneth N Vanderpuye/

Supervisory Patent Examiner, Art Unit 2613